REMARKS/ARGUMENTS

Reconsideration of the rejections set forth in the Office Action dated January 21, 2004 is respectfully requested. Claims 1-40 and 42-53 have been rejected. Claim 41, which had been objected to, has been canceled. As such, claims 1-40 and 42-53 are currently pending.

Claims 34 and 35 have been amended to maintain consistency from their base claim which recites a computer program.

Claims 40 and 43 have been amended to include a limitation recited in claim 41, as originally filed. Current claims 44-53 have been amended to compensate for an error in the numbering of the originally filed claims, in accordance with the Examiner's instructions as set forth in the Office Action dated January 21, 2004. Claims 48-50 and 53 have further been amended such that their dependencies are consistent with their renumbered base claims.

Allowable Subject Matter

Claim 41 was objected to as being dependent upon a rejected base claim. The Examiner indicated in the Office Action dated January 21, 2004, that claim 41 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In response to the Examiner's objection, the Applicants have incorporated the limitation of claim 41 into its base claim (claim 40), and have cancelled claim 41. Accordingly, it is believed that claim 41 is now allowable over the art of record.

Claim Objections

Claims 34 and 35 have been rejected by the Examiner for informalities. In response to

the Examiner's objections to claims 34 and 35, the Applicants have amended claims 34 and 35 to recite computer programs rather than methods. Accordingly, the Applicants submit that the Examiner's claim objections have been overcome.

Rejections under 35 U.S.C. § 102

The Examiner has rejected claims 1-5, 7, 9, 10, 19-25, 29-34, 36-38, and 44-53 under 35 U.S.C. § 102(e) as being anticipated by Francis et al. (U.S. Patent No. 6,580,720).

1. Independent Claim 1 and its dependents

Independent claim 1 requires that an apparatus for maintaining a data circuit includes a plurality of interface cards, a cross-connect unit, a control unit, and a backplane. The cross-connect unit is based on an associated matrix which identifies the interface cards that will receive a data stream and the order in that the interface cards will receive the data stream.

The Examiner has argued that Francis et al. disclose the system of claim1. The Examiner has stated that he is of the position that information about all possible paths is an associated matrix (Office Action dated January 21, 2004, page 3), and that when Francis et al. select a lowest latency path that is available, Francis et al. somehow anticipate the apparatus of claim 1.

The Applicants respectfully disagree with the Examiner's reasoning that Francis et al. teach the apparatus of claim 1. Claim 1 specifically requires that an associated matrix identifies the **interface cards that will receive a data stream** and an **order that the interface cards will receive the data stream**. Hence, more than one interface card will receive the data stream, and not only does the associated matrix identify the interface cards that will receive the data stream, the associated matrix also identifies an order in which the interface cards will receive the data stream.

Contrary to the Examiner's statements, Francis et al. do not appear to teach of an

associated matrix that identifies interface cards that will receive a data stream as well as an order that the interface cards will receive the data stream. In the passages of Francis et al. that are cited by the Examiner, Francis et al. teach that an MIPPSS locates a lowest latency path to achieve a connection (Francis et al., column 39, lines 2-4). If the lowest latency path is not available, the MIPPSS locates the next lowest latency connection (Francis et al., column 39, lines 4-7). A controller determines the latency of all possible signal paths and selects the lowest latency signal path for each connection that it determines is presently available (Francis et al., column 40, lines 41-60). It is respectfully submitted that Francis et al. appear to teach of determining the latency of a plurality of paths, and identifying a single path for each connection based on which available path has the lowest latency. Determining the latency of a plurality of paths, then identifying a single path based on which available path has the lowest latency is **not** equivalent to identifying interface cards that will receive a data stream, and an order that the interface cards will receive the data stream.

There appears to be no teaching or suggestion in Francis et al. of a matrix identifying more than one interface card that will receive a given data stream, or, further, of the matrix identifying an order in which the interface cards will receive the given data stream. Francis et al. specifically teach that only the available path with the lowest latency is used to achieve a connection (Francis et al. column 39, lines 1-12), and neither teaches of nor suggests that a data stream will by more than one interface card in an order determined by a matrix. Therefore, claim 1 and its dependents are each believed to be allowable over Francis et al. for at least this reason.

Claims 2-20 each depend either directly or indirectly from independent claim 1 and are, therefore, each believed to be allowable over the art of record for at least the reason set forth above with respect to claim 1. Each of these claims recites additional limitations which, when considered in the light of claim 1, are believed to further distinguish the claimed invention over the art of record. By way of example, claim 7 requires that each interface card of a plurality of interface cards is connected to all other of the plurality of interface cards through a cross connect unit. The Examiner has stated that Francis et al. disclose that any device can be connected to any other device that uses the same data transfer protocol (Office Action dated January 21, 2004,

page 5), and cited column 37, lines 43-46, of Francis et al. as the basis for his statement. The Applicants note that the passage cited by the Examiner only states that "the present invention provides the ability to interconnect a large number of electronic components in a manner which allows the components to function as if they were physically wired together." It is respectfully submitted that Francis et al. do not teach that each interface card (or I/O port, in the system of Francis et al.) is connected to all other interface cards through a cross connect unit. That is, the ability to interconnect a large number of electronic components does not teach that each I/O port is connected to all other I/O ports of a system. As such, claim 7 is believed to be allowable over Francis et al. for at least this additional reason.

2. *Independent Claim 21 and its dependents*

Independent claim 21 recites an apparatus which includes a plurality of interface cards and a database that contains a matrix for a data circuit. Each interface card in a set of interface cards is receiving a data stream. The matrix identifies the order that a data stream will be routed to a set of interface cards which define a data circuit. A cross-connect unit uses the matrix to determine how to route the data stream, and rotes the data stream to a next destination point when an interface card associated with a destination point becomes inoperable. For each interface card, the matrix includes the destination point and the next destination point.

Claim 21 is believed to be allowable over Francis et al. for at least the reasons set forth above with respect to claim 1. For instance, claim 21 specifically requires that each interface card in a set of interface cards receives a data stream. Francis et al. appear to teach only of forming connections through I/O ports between a sending device and a receiving device (Francis et al. column 40, lines 41-60), and of choosing a single connection based on availability and latency (Francis et al. column 39, lines 1-12). Francis et al. do not appear to teach of a set of receiving devices all receiving a data stream, as required by claim 21. The Applicants are also unable to find any teaching or suggestion in Francis et al. of a matrix that identifies the order that the data stream will be routed to a set of receiving devices. Hence, claim 21 is believed to be allowable over Francis et al.

In his arguments, the Examiner has argued that an interface card is an I/O port (Office Action dated January 21, 2004, page 3). It follows that based on the Examiner's logic, the system of Francis et al. that stores path information would have to store a destination point and a next destination point for each I/O port. The Applicants are unable to find any teaching or suggestion in Francis et al. of storing a destination point and a next destination point for an I/O port. Accordingly, claim 21 is believed to be allowable over Francis et al. for at least this additional reason.

3. Independent Claim 22

Claim 22 recites an apparatus which routes a data stream directly from a first interface card to a third interface card when a second interface card that was supposed to receive the data stream from the first interface card and transmit the data stream to the third interface card becomes inoperable. The apparatus includes a database containing a matrix with a first destination and a second destination for each interface card so that when the second interface card fails, the matrix directs the cross-connect unit to route the data stream from the first interface card to the third interface card.

It is respectfully submitted that claim 22 is allowable over Francis et al. for at least the reasons set forth above with respect to claim 22. In addition, claim 22 requires that when a second interface card that was supposed to receive a data stream from a first interface card and transmit the data stream to a third interface card becomes inoperable, a matrix directs a cross-connect unit to route the data stream from the first interface card to the third interface card. Francis et al. do not appear to teach or suggest that when such a second interface card (an interface card arranged to receive a data stream from a first interface card and to route that data stream to a third interface card) fails, the data stream is still routed from the first interface card to the third interface card. Hence, claim 22 is also believed to be allowable over Francis et al. for this additional reason.

4. Independents Claim 23, 32 and their dependents

Claim 23 recites a method for maintaining a data circuit which includes defining a data circuit as a plurality of interface cards that will receive a particular data stream, and generating a matrix that includes a destination point and a next destination point for each interface card based on the data circuit. The method also includes routing the data stream to appropriate interface cards.

The Applicants submit that, as previously mentioned, Francis et al. do not teach of a plurality of interface cards receiving a data stream. Francis et al. also do not appear to teach of generating a matrix that includes a destination point and a next destination point. Therefore, claim 23 and its dependents are each believed to be allowable over the art of record for at least these reasons.

Claim 32 recites a computer program with code segments for performing the method of claim 23. Accordingly, claim 32 and its dependents are believed to be allowable over Francis et al. for at least the reasons set forth above with respect to claim 23.

5. *Independent Claims 29, 36, and 51*

Claim 29 recites a method for flexibly routing a data stream that includes defining a data circuit as a plurality of interface cards receiving a data stream, and controlling the operation of a cross-connect unit with a matrix, the matrix identifying the order a data stream will be routed to the data circuit including a destination point and a next destination point for each interface card.

As discussed above, Francis et al. do not appear to teach of a plurality of interface cards receiving a data stream, and instead teaches only of sending signals to a receiving device, and not a plurality of receiving devices. Francis et al. also do not appear to teach of a matrix identifying the order a data stream will be routed that includes a destination point and a next destination point. Therefore, claim 29 is believed to be allowable over Francis et al. for at least these reasons.

Claim 36 recites a computer program with code segments for performing the method of claim 29. Claim 51 recites an apparatus with means for performing the method of claim 29. Accordingly, claims 36 and 51 are believed to be allowable over Francis et al. for at least the reasons set forth above with respect to claim 29.

6. Independent Claims 30, 37, 52 and their dependents

Claims 30, 37, and 52 recite generating a matrix that identifies interface cards to receive a data stream and includes destination and next destination points for each interface card. In each of these claims, a data stream is transmitted from a first interface card to a third interface card when a second interface card which was planned to **receive the data stream from the first interface card and transmit the data stream to the third interface card** is rendered inoperable.

It is respectfully submitted that Francis et al. does not appear to teach of a system in which the inoperability of a second interface card which was planned to receive a data stream from a first interface card via a cross-connect unit and to transmit the data stream to the third interface card causes the data stream to be routed from the first interface card through the cross-connect unit to the third interface card. The Applicants are unable to find any teaching in the passages of Francis et al. cited by the Examiner of effectively bypassing a second interface card which was to route a data stream from a first interface card to a third interface card and routing the data stream from the first interface card to the third interface card. It does not appear that Francis et al. even contemplates a system in which a second I/O port (which the Examiner seems to have equated to interface cards) is arranged to route a signal to a third I/O port unless the second I/O port is inoperable, in which case the second I/O port is bypassed. Hence, claims 30, 37, 52, and their dependents are believed to be allowable over Francis et al. for at least this reason.

7. Independent Claims 44 and 45

Claim 44 recites a method for establishing a virtual intelligent backplane. The method includes connecting a plurality of interface cards to each other, establishing a mapping table for a data circuit, determining that a first interface card connected to a second interface card and a third interface card is inoperable, and connecting the second interface card to the third interface card when the mapping table defines the third interface card as a next connection for the second interface card.

Contrary to the Examiner's assertions in the Office Action dated January 21, 2004, it does not appear that Francis et al. disclose determining that a first interface card connected to a second interface card and a third interface card is inoperable, and connecting the second interface card to the third interface card when a mapping table defines the third interface card as a next connection for the second interface card. Assuming, for the sake of argument, that a first interface card is a receiving I/O port of a next lowest latency path, a second interface card is a sending I/O port, and a third interface card is a receiving I/O port of a lowest latency path that is not selected (Office Action dated January 21, 2004, page 10), there is no teaching or suggestion in Francis et al. that the first interface card (receiving I/O port of a next lowest latency path) is connected to the third interface card (receiving I/O port of a lowest latency path that is not selected). Therefore, claim 44 is believed to be allowable over Francis et al. for at least this reason.

In addition, Francis et al. also do not appear to teach of connecting a second interface card (sending I/O port) that is connected to a first interface card (receiving I/O port of a next lowest latency path) to a third interface card (receiving I/O port of a lowest latency path that is not selected), where the third interface card is also connected to the first interface card. Hence, claim 44 is believed to be allowable over Francis et al. for at least this reason as well.

Claim 45 recites similar limitations to those recited in claim 44. As such, claim 45 is believed to be allowable over Francis et al. for at least the reasons set forth with respect to claim 44.

Rejections under 35 U.S.C. § 103

The Examiner has rejected claims 6, 8, 11-18, 27-29, 35, 39, 40, 42, 43, and 50 under 35 U.S.C. § 103(a) as being unpatentable over Francis et al.

As amended, independent claims 40 and 43 recite defining a circuit mapping table which includes information relating to how interface cards are connected together through a cross-connect, detecting when one or more of the interface cards is disconnected from the cross-connect, and connecting the remaining interface cards together through the cross-connect based on information contained in the circuit table. Claims 40 and 43 also recite that at least a first one of the remaining interface cards was connected to at least a second one of the remaining interface cards through the one or more disconnected cards prior to the one or more interface cards becoming disconnected from the cross-connect.

As claim 40 and 43 each now include a limitation which the Examiner indicated was allowable in the Office Action dated January 21, 2004. Claim 40, claim 42 (which depends from claim 40), and claim 43 are each now believed to be allowable over the art of record.

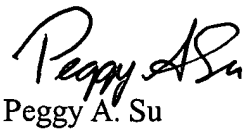
Claims 6, 8, 11-18, 27-29, 35, 39, and 50 are each believed to be allowable over Francis et al. for at least the reasons set forth above with respect to their respective base claims.

Conclusion

In view of the above, the Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below. If any fees are due in connection with the filing of this amendment, the Commissioner is authorized to charge such

fees to Deposit Account 50-1652 (Order No. CISCP795).

Respectfully submitted,



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